**Two-Layer ITO Metallization in Transparent Electronics**

D. S. Memikoglu1, M. Ekström2, P. E. Hellström3,

*1,2,3 KTH Royal Institute of Technology, Stockholm, Sweden*

**Introduction**

Enabling invisible electronics requires that both transistors and interconnects are transparent in the visible spectrum [1]. Interconnects made of ITO offer >80% transparency in the visible range and a resistivity of ~100 μΩcm [2]. Currently, ITO is used as large-area electrodes, e.g., in solar cells, and typically patterned by wet etching. For metal pitch <10 µm, typically found in integrated circuits, dry etching is required. This study presents several key processes for implementing a two-layer ITO metallization scheme within a CMOS platform, with a focus on dry etching of ITO. These processes provide a way of fabricating transparent circuits.

**Experiments & Results**

ITO was deposited on thermally oxidized 100 mm silicon wafers with dc magnetron sputtering. Forming gas anneal (FGA) of ITO at 450 °C yielded sheet resistance of ~5 Ω/sq (400 nm). ITO is patterned with I-line stepper lithography. An ICP-RIE process with CH4/Cl2/H2 chemistry and SiO2 hard mask was developed, enabling well-defined ITO layers with a 4 µm metal pitch (Tab. 1). The two-layer ITO metallization was evaluated with contact chain structures. I‑V measurements across 120 chips demonstrated average contact resistance of ~85 Ω (Fig. 1). The compatibility of TiW/Al or TiN/Al to ITO was evaluated for the fabrication of measurement pads to provide external connections. While the measured resistance between TiW/Al and ITO was low (~3-5 Ω), metal delamination was observed in SEM after FGA (Fig. 2). TiN/Al on ITO was intact after FGA, albeit with higher resistance (~6-8 Ω).

**Conclusions**

A process to define 2 µm half-pitch ITO interconnects using dry etching has been established. Two-level metallization was evaluated by contact chains. The compatibility of TiW/Al and TiN/Al to ITO layer was investigated.

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| **Table 1.** ICP-RIE details of ITO etch | **(a) (b)**  **Figure 1.** (a) Schematic illustration of ITO to ITO contact experiment. (b) ITO to ITO contact resistance for 120 chips (RAVG = 85 Ω) |
| **(a) (b) (c) (d)**  **Figure 2.** (a) Schematic illustration of TiW/Al or TiN/Al to ITO wafers. I-V results of (b) TiN/Al to ITO contact (c) TiW/Al to ITO contact. (d) Metal delamination of TiW/Al in SEM, the metal film burst from probing. | |
| **References**  [1] G. Thomas, Nature, vol. 389, pp. 907-908, 1997.  [2] K. Ellmer, Nat. Photonics, vol. 6, pp. 809-817, 2012 | **Acknowlegments**  This work was partly funded by Vinnova through Advanced Chip Technologies (grant 2023-00543), Swedish Foundation for Strategic Research (SSF RIF 2) and myfab. |